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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,073	02/25/2004	Teruo Takizawa	118439	8936

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EXAMINER


QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/785,073	Applicant(s) TAKIZAWA, TERUO	
	Examiner Kevin Quinto	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, and 4-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 9 are rejected under 35 U.S.C. 102(a, b) as being anticipated by Taguchi et al. (JP 05-175536).
4. In reference to claim 1, Taguchi et al. (JP 05-175536, hereinafter referred to as the "Taguchi" reference) discloses a device which meets the claim. Figure 8 of Taguchi discloses a diode with a p-type silicon layer (4) containing germanium and an n-type silicon layer (6) junctioned to the p-type silicon layer (4). The n-type silicon layer (6) is disposed on an insulating substrate (1a).
5. With regard to claim 9, the p-type silicon layer (4) and the n-type silicon layer (6) are contacting the insulating substrate (1a).

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6. Claims 2, 7, 10, and 11 are rejected under 35 U.S.C. 102(a, b) as being anticipated by Taguchi et al. (JP 05-175536).
7. In reference to claim 2, Taguchi (JP 05-175536) discloses a device which meets the claim. Figure 8 of Taguchi discloses a diode with a p-type silicon layer (4) containing germanium. An intrinsic silicon layer (indicated by "I" in the figures) is junctioned to the p-type silicon layer (4). An n-type silicon layer (6) is junctioned to the intrinsic silicon layer (4).
8. With regard to claim 7, the diode is disposed on an insulating substrate (1a).
9. With regard to claim 10, the p-type silicon layer (4), the n-type silicon layer (6), and the intrinsic silicon layer are disposed on an insulating substrate (1a).
10. With regard to claim 11, the p-type silicon layer (4), the n-type silicon layer (6), and the intrinsic silicon layer are contacting the insulating substrate (1a).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (JP 05-175536) as applied to claim 1 above and further in view of Beasom (United States Patent Application Publication No. US 2003/0071291 A1) and further in view of Shopbell (USPN 6,055,460) and further in view of Farber et al. (USPN 6,187,684 B1).

13. In reference to claim 6, figure 8 of Taguchi discloses a diode with a p-type silicon layer (4) containing germanium and an n-type silicon layer (6) junctioned to the p-type silicon layer (4). Taguchi does not disclose forming the silicon-germanium mixed crystal by implanting germanium to the p-type silicon layer. However this method of forming silicon germanium is well known in the art. Beasom (United States Patent Application Publication No. US 2003/0071291 A1) discloses that using ion implantation (implanting germanium into silicon) in order to form silicon germanium is a known method (p.4, paragraph 39). Furthermore Shopbell (USPN 6,055,460) discloses that ion implantation has the benefit of taking place in a clean environment (column 6, lines 35-38). Farber et al. (USPN 6,187,684 B1, hereinafter referred to as the "Farber" reference) discloses that fabrication in a clean environment is desired in the semiconductor art (column 2, lines 23-26). In view of Beasom, Shopbell, and Farber, it would therefore be obvious to utilize ion implantation as the means of forming the silicon germanium mixed crystal.

14. Claims 1, 4, 5, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (United States Patent Application No. US 2003/0197598 A1) in view of Taguchi et al. (JP 05-175536) and further in view of DiPiazza (United States Patent Application Publication No. US 2003/0137284 A1) and further in view of Streetman ("Solid State Electronic Devices," p. 205).

15. With regard to claim 1, Hayashi (United States Patent Application No. US 2003/0197598 A1) discloses a similar device. Figures 9 and 10 of Hayashi disclose a semiconductor device with a bridge rectifier circuit (3 in figure 9, figure 10 has added detail) having a plurality of diodes (D1-D4, figure 10). Hayashi does not disclose the

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use of a diode which uses a p-type silicon layer containing germanium and an n-type silicon layer junctioned to the p-type silicon layer with n-type junction layer disposed on an insulating substrate. However the use of such diodes is well known in the art.

Taguchi (JP 05-175536) discloses a PIN diode in figure 8 with a p-type silicon layer (4) containing germanium and an n-type silicon layer (6) junctioned to the p-type silicon layer (4). The n-type silicon layer (6) is disposed on an insulating substrate (1a).

DiPiazza (United States Patent Application Publication No. US 2003/0137284 A1) states that PIN diodes are known to have a fast switching time (p.1, paragraph 4).

Streetman ("Solid State Electronic Devices," p. 205) states that diodes with a fast switching speed are desirable in the art. In view of DiPiazza and Streetman, it would therefore be obvious to implement the Taguchi diode in the bridge rectifier circuit of Hayashi.

16. In reference to claim 4, the bridge rectifier circuit (3, figure 9) of Hayashi has a plurality of diodes (D1-D4, figure 10) which rectify a predetermined alternating-current voltage to a direct-current voltage.

17. With regard to claim 5, figure 9 of Hayashi shows that the semiconductor device has a coil antenna (L1) coupled to one side of the bridge rectifier circuit (3); a smoothing capacitor (Ca) coupled to the other side of the bridge rectifier circuit (3). The coil antenna (L1) generates an alternating-current voltage by electromagnetic induction. The bridge rectifier circuit (3) rectifies the alternating-current voltage into a direct-current voltage. The smoothing capacitor (Ca) smoothes the direct-current voltage into a constant voltage.

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18. With regard to claim 9, the p-type silicon layer (4) and the n-type silicon layer (6) are contacting the insulating substrate (1a).

19. Claims 2, 7, 8, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (United States Patent Application No. US 2003/0197598 A1) in view of Taguchi et al. (JP 05-175536) and further in view of DiPiazza (United States Patent Application Publication No. US 2003/0137284 A1) and further in view of Streetman ("Solid State Electronic Devices," p. 205).

20. With regard to claim 2, Hayashi (United States Patent Application No. US 2003/0197598 A1) discloses a similar device. Figures 9 and 10 of Hayashi disclose a semiconductor device with a bridge rectifier circuit (3 in figure 9, figure 10 has added detail) having a plurality of diodes (D1-D4, figure 10). Hayashi does not disclose the use of a diode which uses a p-type silicon layer containing germanium and an n-type silicon layer junctioned to the p-type silicon layer with n-type junction layer disposed on an insulating substrate. However the use of such diodes is well known in the art. Taguchi (JP 05-175536) discloses a PIN diode with a p-type silicon layer (4) containing germanium. An intrinsic silicon layer (indicated by "I" in the figures) is junctioned to the p-type silicon layer (4). An n-type silicon layer (6) is junctioned to the intrinsic silicon layer (4). DiPiazza (United States Patent Application Publication No. US 2003/0137284 A1) states that PIN diodes are known to have a fast switching time (p.1, paragraph 4). Streetman ("Solid State Electronic Devices," p. 205) states that diodes with a fast switching speed are desirable in the art. In view of DiPiazza and Streetman, it would

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therefore be obvious to implement the Taguchi diode in the bridge rectifier circuit of Hayashi.

21. With regard to claim 7, the diode is disposed on an insulating substrate (1a).

22. In reference to claim 8, the bridge rectifier circuit (3, figure 9) of Hayashi has a plurality of diodes (D1-D4, figure 10) which rectify a predetermined alternating-current voltage to a direct-current voltage.

23. With regard to claim 10, the p-type silicon layer (4), the n-type silicon layer (6), and the intrinsic silicon layer are disposed on an insulating substrate (1a).

24. With regard to claim 11, the p-type silicon layer (4), the n-type silicon layer (6), and the intrinsic silicon layer are contacting the insulating substrate (1a).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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KVQ



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